La Recherche d'IBM va travailler avec les leaders de l'industrie et des universités européennes afin d'améliorer le temps de production, le coût et la fiabilité des puces électroniques

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IBM Research and European Union Aim to Greatly Improve Chip Design Time, Cost and Reliability

Pioneering project will lay the groundwork for cost savings alongside efficient high level design methodologies and tools

February 12, 2010 -- IBM Research today announced its collaboration with industry leaders and universities in the European Union to improve the productivity and reliability of semiconductor and electronic systems design. By providing a systematic methodology and an integrated environment for the diagnosis and correction of errors, the EU-funded DIAMOND consortium expects to slash design time and enable significant savings per chip.

"*Designing a microelectronic chip is very expensive and the design costs are the greatest threat to continuation of the semiconductor industry's phenomenal growth*," noted **Dr. Jaan Raik, senior researcher** at Tallinna Tehnikaülikool and coordinator of the DIAMOND project. "*The increasing gap between the complexity of new systems and the productivity of system design methods can only be mitigated by developing new and more competent design methods and tools*."

The new integrated approach will localize and correct bugs on all abstraction levels, from specification through implementation down to the silicon layout. Handling this full chain of levels will allow the solution to take advantage of hierarchical diagnosis and correction capabilities incorporating a wide range of error sources.

"*Correctness, already one of the major showstoppers for design, is becoming ever harder to attain*," explained **Cindy Eisner, senior technical staff member** at IBM Research – Haifa and partner in the DIAMOND consortium. "*Better debugging techniques must be a major focus in research and development if we want to keep increasing the scale of electronics design*."

Today, approximately 70% of design efforts are dedicated to verification and debugging. Two thirds of this is dedicated to discovering and localizing the source of the fault and then correcting it. Another threat is the rapidly growing rate of soft errors, which are transient errors caused, for example, by

cosmic radiation. Soft errors cannot be corrected after the fact, but they can be dealt with by dedicated detection logic, and measuring robustness of that logic can be dealt with by techniques used for detecting other types of errors. The goal of the DIAMOND consortium is to address these challenges and cut fault localization and correction efforts in half – thereby reducing design time by 23%.

According to estimates, fault localization and correction for each chip is expected to cost 34.5 million dollars per chip by 2010. With DIAMOND aiming to reduce this time by 50%, it has the potential to cut design costs by an estimated 17.25 million dollars per chip. Reducing the time spent finding and fixing bugs will also result in significantly shorter design cycle and lower costs as well as shorter time to market.

Using a holistic approach, the DIAMOND consortium will develop new tools and methodologies to help track these errors. Through the incorporation of advanced high performance technology and analytics, the approach will generate millions of 'guesses' on where the bugs might originate, filter out the good ideas and eliminate the bad ones, test the reasonable ideas and then offer verification engineers guidelines on how to find and correct the errors.

By 2011, there will be over 16 billion embedded devices in operation worldwide or 3 devices to every human being on earth. These numbers make finding a better way to correct faults critical for the industry.

The Diamond consortium launched a three-year project this month. The consortium partners include the IBM Research - Haifa, Israel; Ericsson, Sweden; Tallinna Tehnikaülikool, Estonia; Linköpings Universitet, Sweden; Universität Bremen, Germany; Technische Universität Graz, Austria; TransEDA Systems, Hungary; Testonica Lab, Estonia

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